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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,834	12/27/2001	Brett W. Murdock	1280.SC11318TH	9616

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EXAMINER	
ROJAS, MIDYS	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,834	MURDOCK ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7 and 11-15* is/are allowed.

6)☒ Claim(s) *1-6,8-10 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

AT

DETAILED ACTION

Response to Arguments

In view of applicant's remarks, filed on August 30th, 2005, the finality of the last office action is hereby withdrawn and a new ground of rejection is presented.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim1-5, 7-10, 16-19, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lary et al. (2003/0065893) in view of Zitlaw (US 2003/0046485 A1).

Regarding Claim 1, Lary discloses a method comprising:

when in a first mode of operation (first state), utilizing a first output (control line) coupled to a memory (through MUX 302) to provide a first data lane enable for facilitating access of a portion of a first memory storage location of the memory associated with a first memory address (first value is asserted... firmware access is enabled as shown by line 310, see Figure 3, and paragraphs 20, 23-24); and

when in a second mode of operation (second state), utilizing the first output (control line) to provide an address bit of a second memory address for facilitating designation of a second memory storage location of a memory (second value is asserted... firmware access is enabled as shown by line 316, see Figure 3, and paragraphs 23-24). Since firmware access is enabled for the access of memory 212, the service processor may read and/or write to this selected memory

(see paragraph 16) and both of these accesses require providing a memory address for the designation of a memory location for such operation.

Lary does not teach the first and second non-volatile memories (230 and 212) being part of one memory unit. Zitlaw discloses a non-volatile memory array 102 composed of multiple non-volatile memory units (Figure 1 and paragraph 0013). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Lary so that the non-volatile memories 212 and 230 were part of a single memory unit as shown by Zitlaw since implementing memories in array format are known to provide more reliability at a lower cost.

Claim 16 is rejected using the same rationale as that of claim 1, wherein the first register is part of service processor 226 and the output to indicate a first or second mode (first or second state) is equivalent of a value that is asserted;

The address control portion is equivalent to south bridge controller 204, which controls the access of memory 230 when in a first mode of operation (first state);

The first data lane enable control portion is equivalent to MUX 304, which depending on the value asserted and the mode of operation, acts as a switch to enable the access of memory 212 when in a second mode of operation (see Figure 3);

Output 228 is coupled to memory 230 and output 210 is coupled to memory 212.

Claim 19 is rejected using the same rationale as that of claim 1 wherein the processing module is represented by service processor 226, which, as a common processor, must have an internal memory for the storage of operational programming instructions.

Claim 21 is rejected using the same rationale as that of claim 1 wherein the microcomputer is represented by service processor 226.

Regarding Claims 2-4, Lary discloses accessing external memories 230 and 212 wherein the memories being accessed are different memories (as shown in Figure 3). Since the different memories are being accessed independently in different accessing modes (or states), the system is accessing independent memories, which can be of different widths (byte wide or word wide). Additionally, since a word (i.e. 16 or 32) is always bigger than a byte (which is 8 bits) it is understood that a word wide memory has more than 8 bits associated with it.

Regarding Claim 5, Lary discloses the first output being the first output (control line) of a first device (226); and the first and second modes of operation utilize the first output to access a second device (230 or 212) external to the first device.

Regarding Claims 8 and 9, Lary discloses determining a mode of operation to be one of a first mode of operation and a second mode of operation (see paragraph 23). This is done via the assertion of a value (register value), which enables the selection of one of the two memory devices (230 or 212).

Regarding Claim 10, Lary discloses the method further comprising: when in the first mode of operation, utilizing a second output to provide an address bit of the first memory address for facilitating designation of the first memory storage location. Since firmware access is enabled for the access of memory 230, the service processor may read and/or write to this selected memory (see paragraph 16) and both of these access require providing a memory address for the designation of a memory location for such operation;

when in the second mode of operation, utilizing the second output to provide a second data lane enable for facilitating access of a portion of the second memory storage location associated with the second memory address (second value is asserted... firmware access is enabled as shown by line 316, see Figure 3, and paragraphs 23-24).

Regarding Claim 17, Lary discloses the apparatus further comprising a multiplexor (302, 304) having a control input (line 306) coupled to the output of the first register (in 226), a first data input coupled to the address control pin (connection to south bridge 204), a second data input coupled to the first data lane enable (enabling access of 212 in second state through bus 308), and an output coupled to the output pin (outputs coupled to busses 228 or 210).

Regarding Claim 18, Lary discloses the apparatus wherein the first register (in 226) is associated with one of a plurality of chip selects wherein chip selects are associated with the value that is asserted for the selection of one of the two memories (230 or 212).

3. Claims 6, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lary et al. (2003/0065893) in view of Zitlaw (2003/0046485) and further in view of Microsoft Computer Dictionary, where the Microsoft Computer Dictionary is used as an evidentiary reference.

Regarding Claims 6 and 20, Lary in view of Zitlaw disclose the invention as set forth by claims 5 and 19 above. Lary in view of Zitlaw does not teach a third mode of operation in which the system accesses internal storage. Since computer systems (such as that of processor 226) are known to have internal primary storage for their direct access (Main Memory, see Microsoft Computer Dictionary, Page 355), it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into system of Lary in view of Zitlaw the use of a

third mode of operation for tracking internal primary storage accesses, thus allowing the system to more accurately monitor accesses to all available storage.

Allowable Subject Matter

4. Claims 7, 11, 12, 13, 14, and 15 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 7, the Prior Art of Record does not teach nor suggest in the claimed combination an address bit used to extend an address range when a memory having a width less than a word is being accessed.

Regarding Claim 11, the Prior Art of Record does not teach nor suggest in the claimed combination a first mode of operation wherein a multiplexing a first set of data provides two least significant bits of a first address, a most significant bit of the first address, and **a lane enable**; while in a second mode of operation multiplexing a second set of data provides two least significant bits of a second address, a most significant bit of the second address, and **two lane enables**; while in a third mode of operation multiplexing a third set of data provides **four lane enables**.

Claims 12-14 are allowed for depending from allowable claim 11.

Regarding Claim 15, the Prior Art of Record does not teach nor suggest in the claimed combination a set of address nodes coupled to one memory wherein different nodes are coupled to the memory for accessing different bit locations within the same memory.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant's amendment filed on February 14th, 2005 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 30th, 2005

Midys Rojas
Examiner
Art Unit 2189

MR

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
10/3/05